IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Sompong P. Olarig et al.	§	Group Art Unit:	2188
Serial No.: 10/039,010	§	Examiner:	Chery, Mardochee
Filed: December 31, 2001	§		
For: Supporting Interleaved Read/Write Operations From/To Multiple Target Devices	§	Atty. Docket:	200304299-1 NUHP:0107/FLE/HOF

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37 C.F.R. 1.8

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July 14, 2006
Date

David M. Hoffman

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Commissioner for Patents
P.O. Box 1450
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Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

In accordance with the OG Notice of July 12, 2005, Applicants respectfully submit this Pre-Appeal Brief Request for Review. This Request is being filed concurrently with a Notice of Appeal. In the Final Office Action mailed May 18, 2006, the Examiner rejected claim 32 under 35 U.S.C. § 102(e) and rejected claims 1-6, 8-11, 13, 16-18, 20-27, 29, and 33-46 under 35 U.S.C. § 103(a). Applicants, however, respectfully submit that these rejections are improper in view of several clear legal and factual deficiencies in the Examiner's rejections.

Independent Claim 32

The Examiner rejected claim 32 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,405,286 to Gupta (hereafter referred to as "the Gupta reference"). Applicants respectfully assert that the Examiner's rejection is legally and factually deficient because several features of independent claim 32 are not disclosed by the Gupta reference. For example, claim 32 recites a computer comprising "a plurality of devices...wherein each of the

devices simultaneously accesses its associated interleaved memory region *in response to a single transaction request.*" (Emphasis added).

From the Final Office Action, it appears that the Examiner is basing the rejection on the fact that Gupta discloses a system in which multiple writes "may occur simultaneously, multiple reads may occur simultaneously, reads and writes may occur simultaneously, and so on." Gupta, col. 6, lines 26-30; *see also* Final Office Action, page 3. However, there is *absolutely no disclosure* in the Gupta reference that these multiple reads and/or writes occur in response to a single transaction. In fact, the Gupta reference actually indicates the opposite. More specifically, the Gupta reference discloses a memory interleaving system that allows *multiple CPUs* to operate simultaneously on different banks of memory. Gupta, col. 6, lines 19-29. Although these multiple CPUs are able to operate in parallel (*i.e.*, simultaneous reads and writes), multiple CPUs, by their very nature, generate multiple transaction requests. In other words, the Gupta reference discloses a many-to-many system and not a system comprising "a plurality of devices...wherein each of the devices simultaneously accesses its associated interleaved memory region *in response to a single transaction request,*" as recited in claim 32. (Emphasis added). In light of this clear deficiency, Applicants respectfully request withdrawal of the pending Section 102 rejection and allowance of claim 32.

Independent Claims 1, 9, 16, and 25

The Examiner also rejected claims 1, 9, 16, and 25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,272,577 to Leung (hereafter referred to as "the Leung reference") in view of U.S. Patent No. 5,761,726 to Guttag (hereafter referred to as "the Guttag reference"). Applicants, however, respectfully assert that several features of independent claims 1, 9, 16, and 25 are not disclosed by either the Leung reference or the Guttag reference, taken alone or in hypothetical combination. For example, independent claim 1 recites a method comprising "*associating* each of the plurality of target devices with a single base address, wherein the same single base address is *associated with each of the plurality of target devices,*" and "sending a multicast transaction to the *single base address* associated with each of the plurality of target devices." (Emphasis added). Independent claim

9 recites a method comprising "accessing a second portion of memory...wherein the first and second portions of memory are *accessed with a single base address* associated with *both* the first target device and the second target device." (Emphasis added). Independent claim 16 recites a computer system comprising "an initiator device...wherein the initiator device is configured to multicast the transaction request to the plurality of target devices *using a single base address...wherein the same single base address* is associated with each of the plurality of target devices." (Emphasis added). Independent claim 25 recites a computer system comprising "an initiator device ...wherein the initiator device is configured to multicast the transaction request to the plurality of target devices *using a single base address* associated with the plurality of target devices..., wherein *the same single base address* is associated with each of the plurality of target devices." (Emphasis added).

The Examiner conceded in the Final Office Action mailed on May 18, 2006, that the Leung reference does not disclose the above-recited claim features and relied on the Guttag reference to teach these features. Final Office Action, page 5. Applicants respectfully assert, however, that the Section 103 rejection is legally and factually deficient, because the Guttag reference does not disclosed the above-recited claim features. The deficiency of the Examiner's rejection of claim 1 is representative of the deficiency of the rejection with regard to independent claims 9, 16 and 25. Accordingly, the deficiency is illustrated through discussion of the Examiner's rejection of claim 1.

In the Final Office Action, the Examiner cited col. 172, lines 48-55 (claim 1) from the Guttag reference to disclose the above-recited claim features. In their entirety, these lines state:

> a plurality of n processors, where n is less than m and each of said n processors has a predetermined *plurality of corresponding memories*, said predetermined plurality of memories corresponding to *each processor having a corresponding fixed base address* within said single memory address space, each of said processors capable of generating any address within said single memory address space for read/write access to data stored within said plurality of m memories.

Guttag, col. 172, lines 48-55 (emphasis added). As the above-quoted section clearly illustrates, the Guttag reference discloses a *plurality* of processors that each have *their own* individual (*i.e., corresponding*) base address within *their own individual section* of the memory address space. *See also*, Guttag, col. 172, lines 43-47 (disclosing a plurality of m memories within the address space, each memory having a "*unique* addressable memory portion"). Consequently, the claim feature "wherein *the same single base address* is associated with each of the plurality of target devices" is the antithesis of uniqueness as taught by Guttag. In light of the clear factual deficiencies of the Examiner's evidence, Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness with regard to claim 1 or claims 9, 16 or 25. Accordingly, Applicants respectfully request withdrawal of the pending Section 103 rejection and allowance of independent claims 1, 9, 16, and 25 and the claims that depend therefrom.

Independent Claims 33 and 36

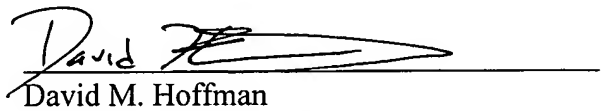
The Examiner rejected independent claims 33 and 36 under 35 U.S.C. § 103(a) as being unpatentable over the Leung, Guttag, and Gupta references. In light of the factual deficiencies of the Leung, Guttag, and Gupta references described above, Applicants respectfully assert that several features of claims 33 and 36 are not disclosed or suggested by the Leung, Guttag, and Gupta references, taken alone or in hypothetical combination with each other. For example, independent claim 33, as amended, recites "associating the plurality of target devices with a single base memory address, *wherein the same single base memory address is associated with each of the plurality of target devices*." (Emphasis added). Independent claim 36, as amended, recites "code to associate the single base address with a plurality of interleaved memory regions, *wherein the same single base address is associated with each of the plurality of interleaved memory regions*." (Emphasis added). For at least the reasons set forth above, Applicants respectfully assert that the above-recited claim features are not taught or suggested by the cited references either alone or in hypothetical combination. Accordingly, Applicants respectfully request withdrawal of the pending Section 103 rejection and allowance of claims 33 and 36, as well as the claims that depend therefrom.

Conclusion

In view of the remarks and amendments set forth above, the Applicant respectfully requests allowance of the pending claims. If the Examiner or the panel believes that a telephonic interview will help speed this application toward issuance, the Examiner or the panel is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: July 14, 2006



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